DEPARTMENT OF COMPUTER SCIENCE (SF)

18UCS102-DIGITAL FUNDAMENTALS AND ORGANIZATION

Unit:1

1. Subtract $(1010)_2$ from $(1101)_2$ using 1st complement.. a)$(1100)_2$ b**)$(0011)_2$** c)$(1001)_2$ d)$(0101)_2$

2. Using 2's Complement, subtraction, of $(1010)_2$ from $(0011)_2$ is

a) $(0111)_2$ b) $(1001)_2$ c**) $-(0111)_2$** d) $-(1001)_2$

3.In 1st Complement a number to be subtracted is known as……

a) **Subtrahend** b) Minuend c) carry d) none of thi

4.In 1st Complement a number which is subtracted from other number Is known

a) Carry b) subtrahend c) **minuend** d) Non of this

5.In a 2nd Complement a number which is subtracted from other Number is known as……..

a) Carry b) **Subtrahend** c) Minuend d) Non of this

6.In 2nd Complement a number which is subtracted from other number Is known as…….

a) Carry b) Subtrahend c**) Minuend** d) on of this

7.The full adder CKT adds. ……Digit at a time

a) 1 b) 2 c) **3** d) 4

8.Full adder is constructed by using …….

a) **Two Half Adder& one OR gate** b) two OR gate &one HA

c) One HA & two OR gate d) One OR gate & one HA 7

9.HA gives……. O/P

a) 1 b) **2** c) 3 d) non of this

10.FA gives…….. O/P

a) 1 b**) 2** c) 3 d) non of this

Unit:2

11.The O/P of Half adder is in the form of.

a) Sum b) carry c**) sum & carry** d) none of these

12.The O/P of Full adder is in the form of ……

a) Sum b) carry c**) sum & carry** d) none of these

13.…….Are used for converting one type of number system in to other form.

a) **Encoder** b) logic gate c) half adder d) FA

14.…… Are used for converting one type of number system in to the other form

a)Decoder b) logic gatec) half adder d) 15.Full adder

77)Multiplexer means ……

a) One in to many b**) many in to one** c) many in to many d) none of these

16.Multiplexers is also known as.

a)mux b) demux c) adder d) subtractor

17.ASCII code is a …… bit code.

a) 1 b) 2 c**) 7** d) **8**

18.8421 codes is also called as.

a) Gray code b) ASCII code c) excess 3-code **d) BCD code**

19.The decimal number is converted in to excess 3 codes by adding. to each decimal

a) 4 b) 8 c) 2 d) **3**

20. The binary system, 1+1=……

(a)2 (b) 0 **(c) 1** (d) none of these

Unit:3

21The access method used for magnetic tape is_____

a) Direct b) Random **c) Sequential** d) None of the above

22.By Processing we understand _____

b) Processing string of only words b**) None of the above** c) String manipulation only

d) Processing string of numbers and special symbols

23.The difference between memory and storage is that the memory is_____ storage is

c) **Temporary, permanent** b) Permanent, temporary c) Slow, fast

d) None of the above

24.Which of the Following holds the ROM, CPU, RAM and expansion cards

d) Hard disk b) Floppy disk **c) Mother board** d) None of the above

25.The language that the computer can understand and execute is called _____

e) **Machine language** b) Application software c) System program

d) None of the above

26.Which of the following devices can be used to directly input printed text

f) **OCR** b) OMR c) MICR d) None of the above

27.A floppy disk contains

g) Circular tracks only b) Sectors only **c) Both circular tracks and sectors**

d) None of the above

28.CD-ROM is a

h) Semiconductor memory b) Memory register c) Magnetic memory

d) None of the above

29.Actual execution of instructions in a computer takes place in

i) **ALU** b) Control Unit c) Storage unit d) None of the above

30.Which of the following is used as a primary storage device

a) Magnetic tape **b) PROM** c) Floppy disk

d) None of the above

unit:4

31.A logic gate is an electronic circuit which

(a) **makes logic decisions** (b) allows electron flow only in one direction

(c) works on binary algebra (d) alternates between 0&1 values

32.In positive logic, logic gate 1 corresponds to

(b) positive voltage **(b) higher voltage level**

(c) zero voltage level (d) lower voltage level

33.In negative logic, the logic state 1 corresponds to

(c) negative logic (b) zero voltage

(c) more negative voltage **(d) lower voltage level**

34.The output of a 2-input OR the gate is 0 only when it's

(d) **both inputs are 0** (b) either input is 1

(c) both inputs are 1 (d) either input is 0

35.An X-OR gate produces an output only when it's two inputs are

(e) high (b) low **(c) different** (d) same

36.An AND gate

(f) implements logic addition **(b) is equivalent to a series switching circuit**

(c) is an any-or-all gate (d)is equivalent to a parallel switching circuit

37.When an input electrical signal A=10100 is applied to a NOT gate, it's output Signal is

(a) 01011 (b) 10101 (c) 10100 (d)00101

38.The only function of a NOT gate is to

(g) stop a signal (b) recomplement a signal

(c) invert an input signal (d) act as a universal set

39.A NOR gate is ON only when all it's inputs are

(h) ON (b) positive (c) high **(d) OFF**

40.The truth table as shown in fig. Is for a/an …… gate.

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

(i) **XNOR** (b) OR (c) AND (d) NAND (e) XOR

Unit:5

41.For getting an output from an XNOR gate, its both inputs must be

(j) high (b) low **(c) at the same logic level** (d) at the apposite logic level

42. Diagram which is used to show logic elements and their interconnections is said to be

A. circuit diagram
B. system diagram
C. logic diagram
D. gate diagram

43. Electrical circuit having all voltages at one of two values are called

A. binary circuit
B. binary logic
C. logic circuit
D. none of the above

44. System with two states is classified as

A. logic
B. binary system
C. binary logic
D. system circuit

45. peration carried out by a NOT gate are also termed as

A. inverting
B. converting
C. reverting
D. reversing

46. Number of logic gates and way of their interconnections can be classified as

A. logical network
B. system network
C. circuit network
D. gate network

47. Logic gate in which any one of inputs is logic 1 results in output as logic 1 is termed as

A. NOT gate
B. NOR gate
C. AND gate
D. OR gate

48. able used to show possible combination of inputs for an output is said to be

A. logic table
B. gate table
C. system circuit table
D. truth table

49. Logic circuit with only one output and one or more inputs is said to be

A. binary gate
B. logic gate
C. circuit gate
D. system gate

50. Table used for result of operation following logical rules is classified as

A. logic gate table
B. circuit gate table
C. truth table
D. system gate table

DEPARTMENT OF COMPUTER SCIENCE (SF)

18UCS102-DIGITAL FUNDAMENTALS AND ORGANIZATION

UNIT:1

1. What Is Digital Logic?

Digital logic is the representation of signals and sequences of a digital circuit through numbers. It is the basis for digital computing and provides a fundamental understanding on how circuits and hardware communicate within a computer.

2. What Is Combinational Logic?

The term combinational logic refers to circuitry that transforms bits, as opposed to storing bits. For example, the ALU portion of a CPU transforms data, e.g. transforming two input word-sized bit strings into an output which is the sum of the two inputs.

3. Explain Sequential Logic?

Sequential logic stores data. Registers in a CPU, RAM and so on store data.

4. **Explain Computer Architecture?**

A modern meaning of the term computer architecture covers three aspects of computer design:

- instruction set architecture.
- computer organization.
- computer hardware.

5. Explain Instruction Set Architecture?

Instruction Set Architecture - ISA refers to the actual programmer-visible machine interface such as instruction set, registers, memory organization and exception handling. Two main approaches: RISC and CISC architectures.

A computer organization and computer hardware are two components of the implementation of a machine. Computer organization includes the high-level aspects of a design, such as the memory system, the bus structure, and the design of the internal CPU (where arithmetic, logic, branching and data transfers are implemented).

Computer hardware refers to the specifics of a machine, included the detailed logic design and the packaging technology of the machine. For many years the interaction between ISA and implementations was believed to be small, and implementation issues were not a major focus in designing instruction set architecture.

In the 1980's, it becomes clear that both the difficulty and inefficiency of pipelining could be increased by instruction set architecture complications.

6. What Are The Tasks Of Computer Architects?

Tasks of Computer Architects : Computer architects must design a computer to meet functional requirements as well as price, power, and performance goals. Often, they also have to determine what the functional requirements are, which can be a major task. Once a set of functional requirements has been established, the architect must try to optimize the design. Here are three major application areas and their main requirements:

Desktop computers: focus on optimizing costperformance as measured by a single user, with little regard for program size or power consumption.

Server computers: focus on availability, scalability,and throughput cost-performance.

Embedded computers: driven by price and often power issues, plus code size is important

7.What Are The Developments Of Computer Design?

Developments in Computer Design : During the first 25 years of electronic computers both forces, technology and innovations in computer design made major contributions. Then, during the 1970's, computer designers were largely dependent upon integrated circuit technology, with roughly 35% growth per year in processor performance.

In the last 20 year, the combination of innovations in computer design and improvements in technology has led sustained growth in performance at an annual rate of over 55%. In this period, the main source of innovations in computer design has come from RISCstyle pipelined processors.

8. Explain Risc Architecture?

RISC Architecture : After 1985, any computer announced has been of RISC architecture. RISC designers focused on two critical performance techniques in computer design: the exploitation of instruction-level the exploitation of instruction level parallelism, first through pipelining and later through multiple instruction issue, the use of cache, first in simple forms and later using sophisticated organizations and optimizations.

9. What Are The Characteristics Of Risc Isa?

RISC ISA Characteristics

- All operations on data apply to data in registers and typically change the entire register;
- The only operations that affect memory are load and store operations that move data from memory to a register or to memory from a register, respectively;
- A small number of memory addressing modes;
- The instruction formats are few in number with all instructions typically being one size;
- Large number of registers;

These simple properties lead to dramatic simplifications in the implementation of advanced pipelining techniques, which is why RISC architecture instruction sets were designed this way.

10. What Is The Main Example Of Cisc Architecture Processor?

Intel IA-32 processors (in over 90% computers). Intel IA-32 processors, from 80386 processor in early 80's to Pentium IV today, and the next one to be introduced this or next year, are of CISC architecture. All Intel IA-32 processors are having as a base the Identical instruction set architecture designed in early 1980's.

UNIT:2

11. What are the five classic components of a computer?

The five classic components of a computer are input, output, memory, datapath, and control.

12. Define – ISA

The Instruction Set Architecture or simply architecture of a computer is the interface between the hardware and the lowest-level software. It includes anything that programmers make a binary machine language program work correctly, including instructions, I/O devices, and so on.

13. Define – ABI

Typically, the operating system will encapsulate the details of doing I/O, allocating memory, and other low-level system functions so that application programmers do not need to worry about such details. The combination of the basic instruction set and the operating system interface provided for application programmers is called the Application Binary Interface (ABI).

14. Define – Response Time

Response time is also called execution time. The total time required for the computer to complete a task, including disk accesses, memory accesses, I/O activities, operating system overhead, CPU execution time, and so on.

15. Define – MIPS

Million Instructions Per Second (MIPS) is a measurement of program execution speed based on the number of millions of instructions.

16. . Define – Addressing Modes

Multiple forms of addressing are generically called addressing modes. The MIPS addressing modes are :

1. Immediate addressing
2. Register addressing
3. Base or displacement addressing
4. PC-relative addressing
5. Pseudo direct addressing

17. Define RAM.
Memory in which any location can be reached in a short and fixed amount of time after specifying its address is called random access memory.

18.Define memory access time.
The time required to access one word is called memory access time.

19.What is instruction register (IR) and program counter (PC) used for ?
The instruction register (IR) holds the instruction that is currently being executed .Its output is available to the control circuits which generate the timing signals that control the various processing elements.

20. What do you mean by memory address register(MAR) and memory data register(MDR)?
The MAR holds the address of the location to be accessed. The MDR contains

UNIT:3

21.What is an interrupt?
Ans: An interrupt is a request from an I/O device for service by the processor. The processor provides the requested service by executing an appropriate interrupt service routine.

22.Explain about Bus.
Ans: Bus is a group of lines that serves as a connecting path for several devices. In addition to the lines that carry the data , the bus must have the lines for address and control purposes.

23.What do you mean by multiprogramming or multitasking?
Ans: The operating system manages the concurrent execution of several application programs to make best possible use of computer resources. This pattern of concurrent execution is called multiprogramming or multitasking.

24. Explain the concept of pipelining.
Ans: Pipelining is the means of executing machine instructions concurrently. It is the effective way of organizing concurrent activity in a computer system. It is a process of substantial improvement in the performance by overlapping the execution of successive instructions.

25. What are the two techniques used to increase the clock rate R?
Ans: The two techniques used to increase the clock rate R are:
1. The integrated – circuit (IC) technology can be increased which reduces the time needed to complete a basic step.
2. We can reduce the amount of processing done in one basic step.

26. What is Big – Endian and Little- Endian representations.
Ans: The Big- endian is used when lower byte addresses are used for the more significant bytes (The leftmost bytes) of the word. The little-endian is used for the opposite ordering, where the lower byte addresses
are used for the less significant bytes (the rightmost bytes) of the word

27. What is indirect addressing mode?
Ans: The effective address of the operand is the contents of a register or memory ocation whose address appears in the instruction

28. What is indexed addressing mode?
Ans: The effective address of the operand is generated by adding a constant value to the contents of a register.

29. Define autoincrement mode of addressing?

Ans: The effective address of the operand is the contents of a register specified in the instruction. After accessing the operand, the contents of this register are automatically incremented to point to the next item in the list.

30. Define autodecrement mode of addressing?
Ans: The contents of a register specified in the instruction are first automatically decremented and are then used as the effective address of the operand.

Unit:4

31. What do you mean by assembler directives?
Ans: These are the instructions which direct the program to be executed. They have no binary equivalent so they are called pseudo-opcodes. These instructions are used to define symbols, allocate space for variable, generate fixed tables etc. Examples : END, NAME

32. What do you man by relative addressing mode?
Ans: The effective address is determined by the index mode using the program counter in place of the general purpose register Ri.
33. What is Stack?
Ans: A stack is a list of data elements, usually words or bytes with the accessing restriction that elements can be added or removed at one end of the list only. It follows last in first out (LIFO) mechanism.

34. What is a queue?
Ans: Is a type of datastructure in which the data are stored in and retrieved on a First in first out(FIFO) basis. It grows in the direction of increasing addresses in the memory. New data are added at the back (High-address end) and retrieved from the front (low-address end) of the queue.

35. What is half adder?
Ans: A half adder is a logic circuit with two inputs and two outputs, which adds two bits at a time, producing a sum and a carry.

36. What is full adder?
Ans: A full adder is logic circuit with three inputs and two outputs, which adds three bits at a time giving a sum and a carry.

37. What is signed binary?
Ans: A system in which the leading bit represents the sign and the remaining bits the magnitude of the number is called signed binary. This is also known as sign magnitude.

38. What are the two approaches used to reduce delay in adders?
Ans:1) The first approach is to use the fastest possible electronic technology in

39. What are the main features of Booth's algorithm?
Ans:
1) It handles both positive and negative multipliers uniformly.
2) It achieves some efficiency in the number of addition required when the multiplier has a few large blocks of 1s.

40.How can we speed up the multiplication process?
Ans: There are two techniques to speed up the multiplication process:
1) The first technique guarantees that the maximum number of summands that must be added is n/2 for n-bit operands.
2) The second technique reduces the time needed to add the summands.

Unit:5

41.Name the methods for generating the control signals.
Ans: The methods for generating the control signals are:
1) Hardwired control
2) Microprogrammed control

42. Define hardwired control.
Ans: Hard-wired control can be defined as sequential logic circuit that generates specific sequences of control signal in response to externally supplied instruction.

43. Define microprogrammed control.
Ans: A microprogrammed control unit is built around a storage unit is called a control store where all the control signals are stored in a program like format. The control store stores a set of microprograms designed to implement the behavior of the given instruction set.

44. What are the major characteristics of a pipeline?
Ans: The major characteristics of a pipeline are:
a) Pipelining cannot be implemented on a single task, as it works by splitting multiple tasks into a number of subtasks and operating on them simultaneously.

45.What is a pipeline hazard?
Ans: Any condition that causes the pipeline to stall is called hazard. They are also called as stalls or bubbles.

46. What are the types of pipeline hazards?
Ans: The various pipeline hazards are:

1. Data hazard
2. Structural Hazard
3. Control Hazard.

47. What is data hazard?
Ans: Any condition in which either the source or the destination operands of an instruction are not available at the time expected in the pipeline is called data hazard.

48.What are the major functions of IO system?
Ans: i. Interface to the CPU and memory through the system bus.
ii. Interface to one or more IO devices by tailored data link.

49.What is an I/O Interface?
Ans: Input-output interface provides a method for transferring binary information between internal storage, such as memory and CPU registers, and external I/O devices

50.Explain Direct Memory Access.
Ans: A modest increase in hardware enables an IO device to transfer a block of information to or from memory without CPU intervention. This task requires the IO device to generate memory addresses and transfer data through the bus using interface controllers.

NGM COLLEGE (AUTONOMOUS) POLLACHI

B.Sc COMPUTER SCIENCE **SEMESTER: I**

18UCS102-Digital Computer Fundamentals and Organization

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Unit-1 K3 Type

1. Convert hexadecimal value 16 to decimal.
2. Convert the following decimal number to 8-bit binary.
3. List the boolean algebra postulates and prove them.
4. What is meant by Excess three codes? Give example.
5. Construct a three bit full subtractor using logic gates.
6. Perform the following subtractions and check the result by connecting the binary number to decimal
   (a)101.101—11.011
   (b) 1011.1 — 100.11
7. What is the ASCII character set? How common is its use?
8. Write the difference between EXCLUSIVE-OR and INCLUSIVE-OR.
9. What is the associativity of the arithmetic operators?
10. Discuss the basic theorems of Boolean algebra.

Unit-II

1. Simplify the following Boolean expression by using Karnaugh map F(A,B,C,D) = A B C + B C D + ABCD + AB C .
2. Describe about the Shift Registers with diagram. Shift Register with diagram.
3. Explain about the synchronous counters with neat diagram and truth table.
4. Reduce the following equation (0,2,3,5,8,10,11,13) m f = S using the McCluskey method.
5. Simplify the following Boolean expression by using Karnaugh map Y(A,B,C,D) = ABCD + AB C D + ABC + AB .
6. Briefly explain about the JK flip-flop with circuit and truth table.

7. Briefly explain about the design of status register.
8. Explain a 1*16 bit multiplexer with truth table.
9. Explain the micro operations of the accumulator.
10. Discuss the programmable logic arrays.

Unit III

1. Analyze the push and pop operations in stack organization
2. Write about the instruction format
3. Differentiate the different types of addressing modes
4. Write a short note on Data Transfer and Manipulation Instructions
5. Differentiate Addition and Subtraction Algorithms for signed magnitude
6. List and Explain the Instruction Formats
7. Explain Data Transfer and Error detection
8. Compare Zero, Single, and Double instruction formats.
9. Analyze the computer organization with neat representation.
10. Write about the different types of address modes in brief.

Unit –IV

1. List and explain the input and output peripherals.
2. Write a short note on Computer input / output interfaces
3. Write a short note on Asynchronous Data Transfer.
4. Discuss the modes of transfer.
5. Explain the priority concept in peripheral devices.
6. Explain about Direct Memory Access.
7. Explain about the input /output processor.
8. Analyze the Memory access methods.
9. List the Peripheral devices that are used for input and output process of data.
10. Analyze the interrupts in the data transfer methods.

Unit V

1.List and explain the memory hierarchy

2. Explain the architecture of main memory in computer organization.

3. Explain the auxillary memory and its advantages.

4. Write short note on Associative memory

5. Write about the cache memory in brief.

6. Explain briefly about the virtual memory.

7. Compare the types of memory by its uses.

8. Analyze the memory organization in brief.

9. Compare the Main memory and Auxillary memory

10. Compare and list the uses of Associative and Cache memory.

DEPARTMENT OF COMPUTER SCIENCE (SF)

18UCS102-DIGITAL FUNDAMENTALS AND ORGANIZATION

Unit – 1

1. Discuss about the Half-subtractors with suitable diagram.
2. Briefly explain about the NAND, NOR and EX-OR gates with detail.
3. Discuss about the Full adder with suitable diagram.
4. Explain the basic and universal logic gates with circuit diagram and truth table. Write note on ALU with details.
5. Explain the universal logic gates with truth table.

Unit-2

1. Discuss briefly the 4-bit input shift register with timing diagram.
2. Simplify the following Boolean expression by using Karnaugh map F(A,B,C,D) = A B C + B C D + ABCD + AB C .
3. Minimize four variables Boolean equation using K-map method
4. Describe the design of the synchronous counter and explain with truth table.
5. Discuss the design of the circuit using PLA with four inputs and four outputs.

Unit-3

1. Explain Stack organization in detail
2. Explain Addressing modes in detail
3. Explain the instruction formats in detail.
4. Describe the design of arithmetic logic unit and their functions.

5. Explain the computer organization in detail.

Unit-4

1. Explain in detail about the peripheral devices involved in data transfer.
2. Explain the Asynchrounous Data Transfer.
3. Explain the Direct Memory Access.
4. Explain about the input/output processor.
5. Explain about the memory organization in computer

Unit-V

1. Explain the memory hierarchy in detail.
2. Explain the architecture of different types of memory in detail.
3. Explain about memory organization
4. Explain detail about the virtual memory.
5. Explain detail about the main memory.